2-STAGE LNA DESIGN

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Introduction

Characteristic	Specification
Operating Frequency	**11.4-12.7G** (Starlink Customer Terminal from Satellite)
Noise Figure	<1 dB (as low as possible)
Insertion Gain (S_{21})	>20 dB (requires 2-stage design)
Output Reflection (S_{22})	<-14 dB
Input Reflection (S_{11})	<-10 dB
Board for hybrid Integration	Duroid 5880 (thickness 10 or 20 mil, ½ oz. Cu)
Active Device to be used	Any of the GaAs FET (non-linear model) from Renesas ADS library, HP ATF36077, Fujitsu HEMT's
Other requirements	Unconditionally stable 0.1-20 GHz

Transistor Selection

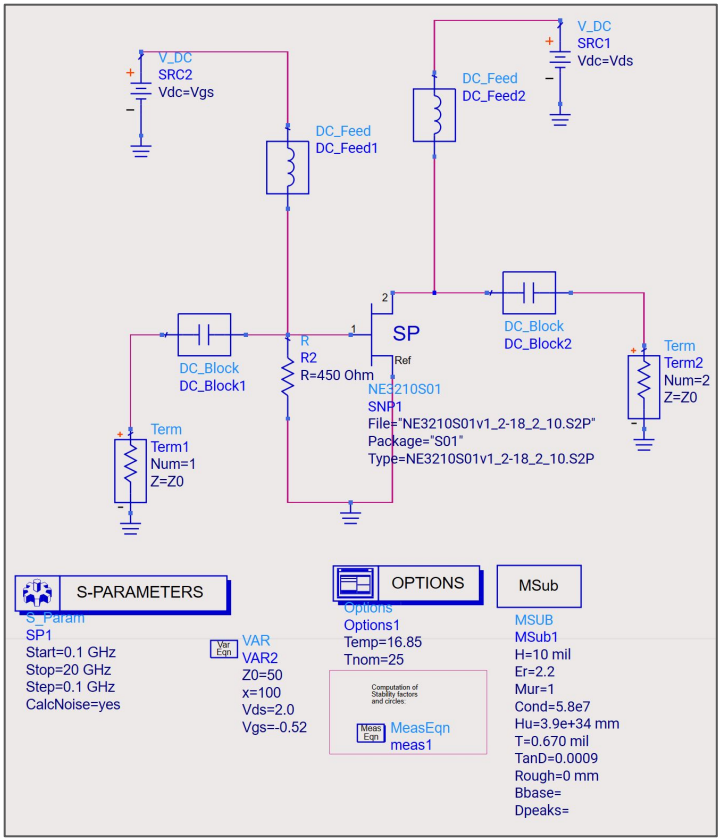
Metric	ATF-36077	FHX04X	NE3210S01	NE3511S02
NFmin(dB)	0.50 dB	0.72 dB	0.34 dB	0.36 dB
Ga(dB)	12 dB	10.5 dB	13.5 dB	12.295 dB

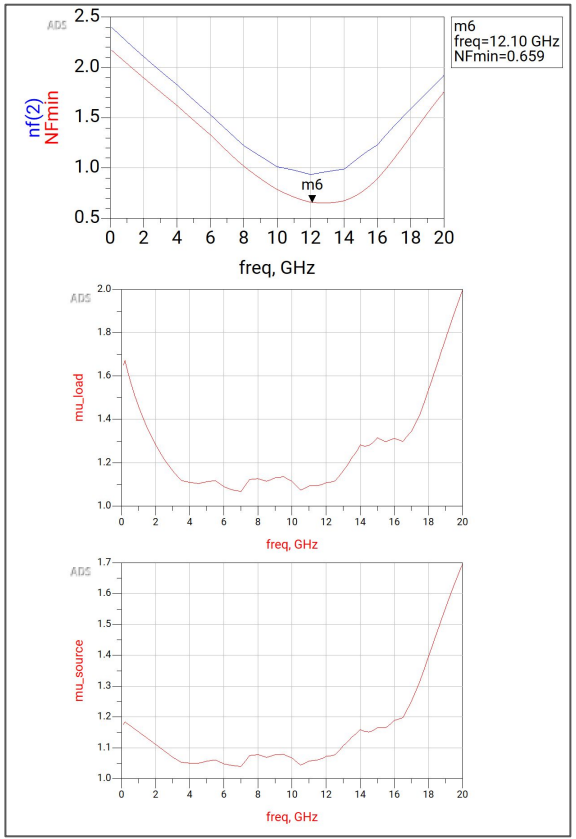
- Evaluated 4 different transistors via their datasheets
- Examined NFmin and associated gain
- Identified target Vds and Ids biases
- NE3210S01 was a clear winner based on its low NFmin @ 12 GHz and high Ga

V_{DS} = 2 V, I_D = 10 mA

Freq. (GHz)	$NF_{min.}$ (dB)	G_a (dB)
2.0	0.25	21.2
4.0	0.26	19.5
6.0	0.28	18.2
8.0	0.30	16.2
10.0	0.32	14.7
12.0	0.34	13.5

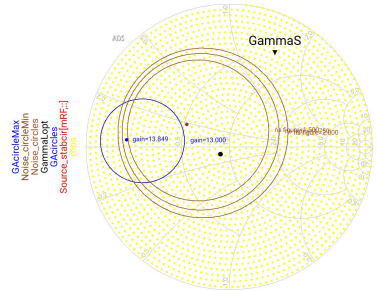
Stabilizing the Transistor





LNA Stage 1 Design Choices

- Based on 10.23 Pozar, the first stage of our LNA dominates the noise budget
- Γopt of the first needs to be precisely matched for NFmin
- Gain can be sacrificed as it will be compensated in the second stage



Move marker m1 to select freq point. All listings and impedances on Smith Chart will be updated.

RF Frequency Selector

m1 0.000 2.00 G 4.00 G 6.00 G 8.00 G 10.0 G 12.0 G 14.0 G 16.0 G 18.0 G 20.0 G

RF Frequency	dB(S11)	dB(S12)	dB(S21)	dB(S22)
12.10 GHz	-6.464	-20.296	11.174	-12.485

Matching For Gain

Zsource — DUT* — Zload

Maximum Available Power Gain, dB	Simultaneous Match Zsource	Simultaneous Match Zload
13.621	8.268 + j2.616	13.080 + j12.333

Stability Factor: 1.121

System Impedance: 50.000

Matching For Noise Figure

NFmin, dB	Zopt for NFmin	Conjugate Match Load Impedance if Source Reflection Coefficient is Sopt for Minimum NF	Power Gain with these Source and Load Reflection Coefficients
0.670	25.8 + j9.27	25.3 + j8.48	12.628

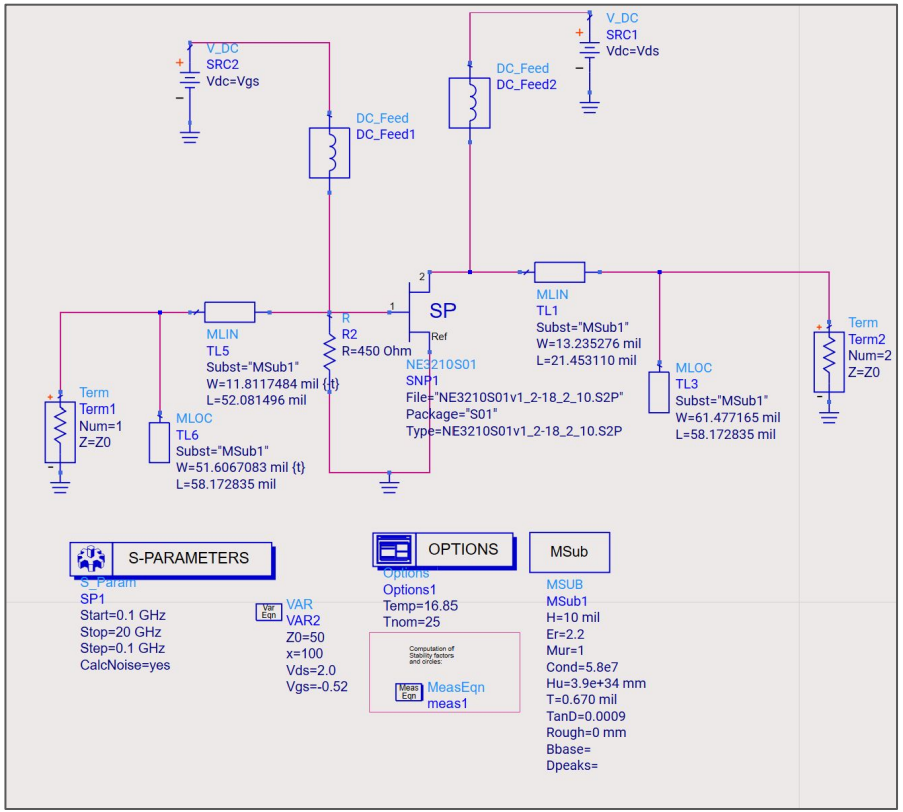
Source Reflection Coefficient for Minimum NF: 0.339 / 152.039

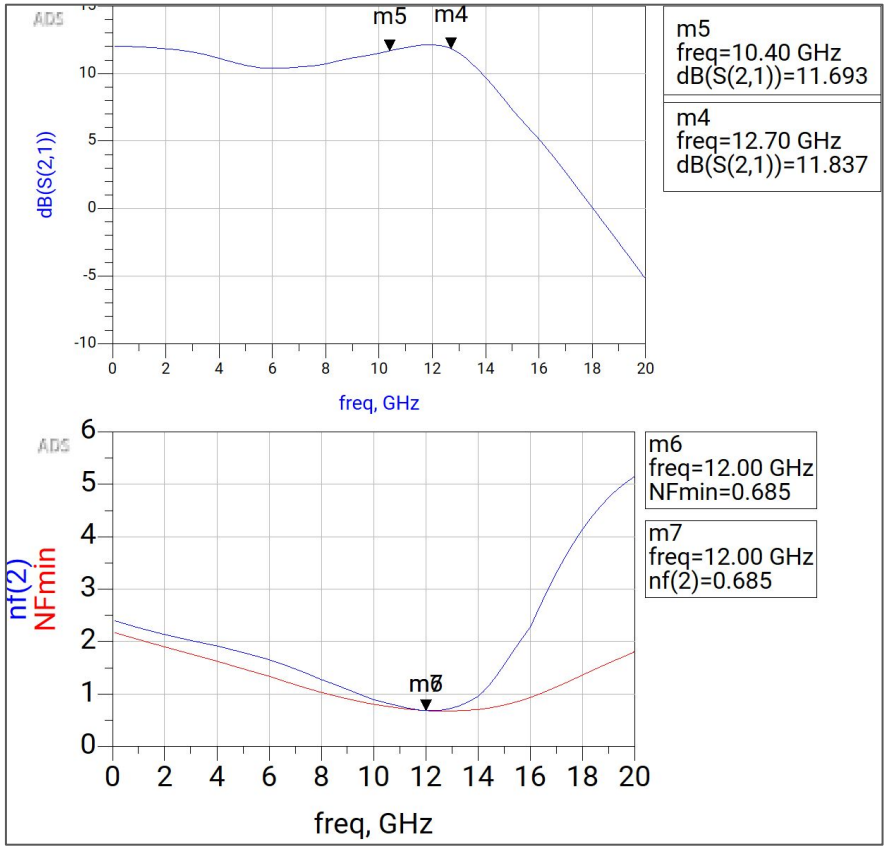
Zopt — DUT* — Conjugate match Zload if source impedance is Zopt

*DUT= Device Under Test (simulated circuit or device)

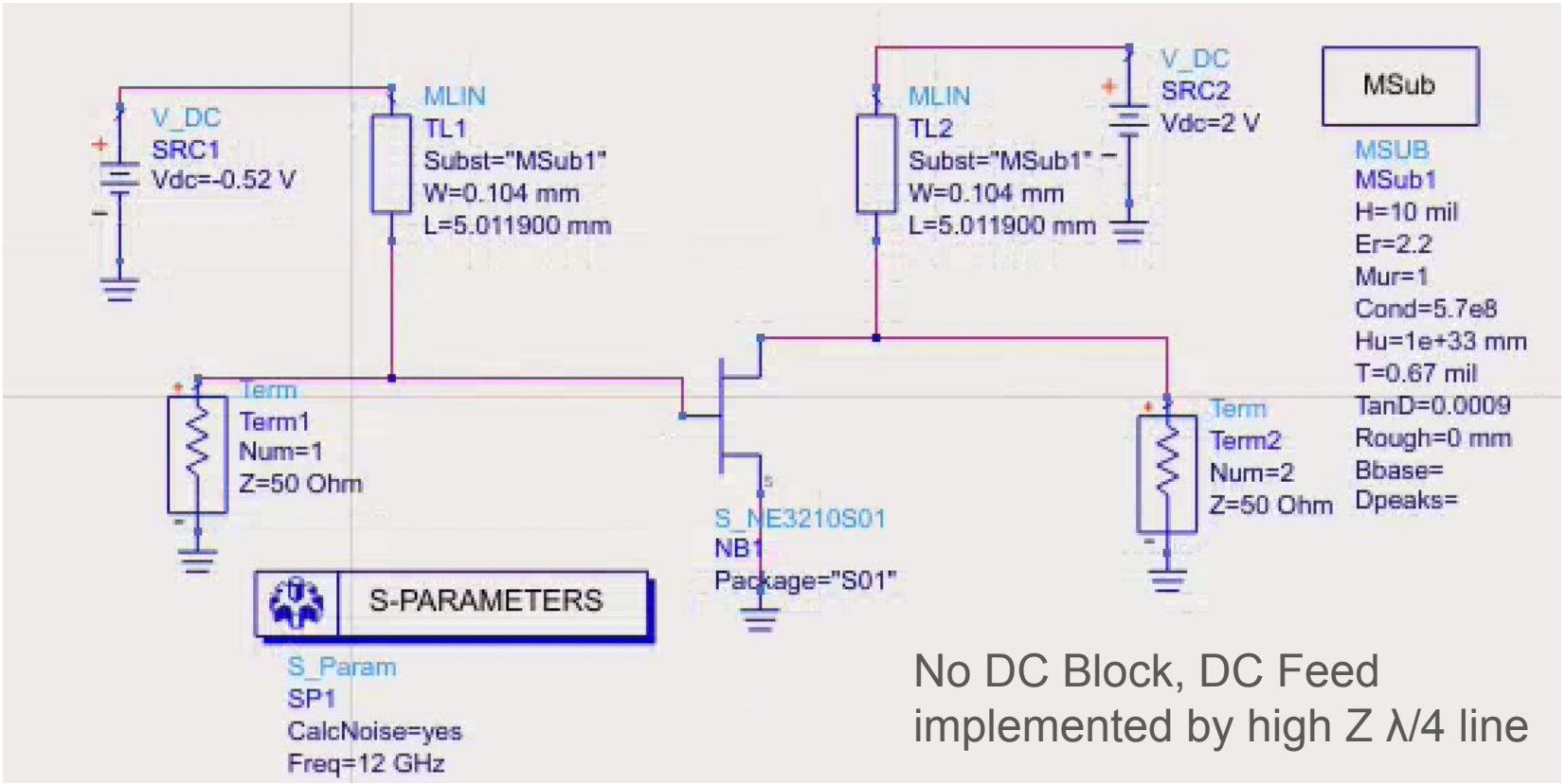
$$F_{\text{cas}} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots . \qquad (10.23)$$

Stage 1 Result





Tentative Stage 2 Design

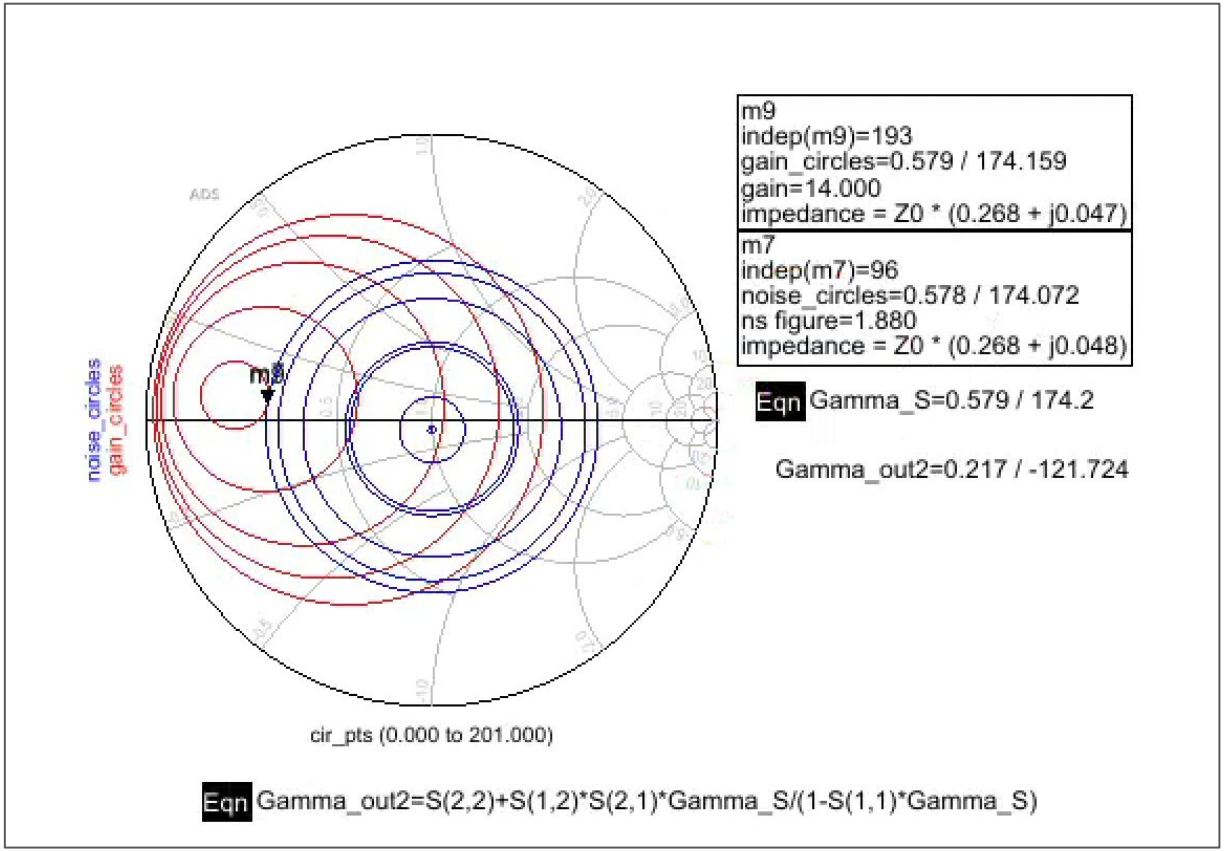


No DC Block, DC Feed implemented by high Z λ/4 line

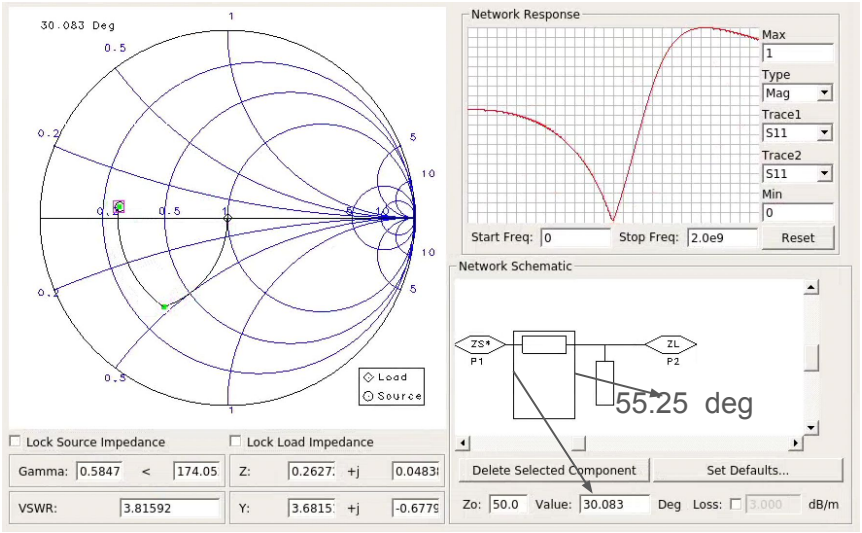
Stage 2 / Matching

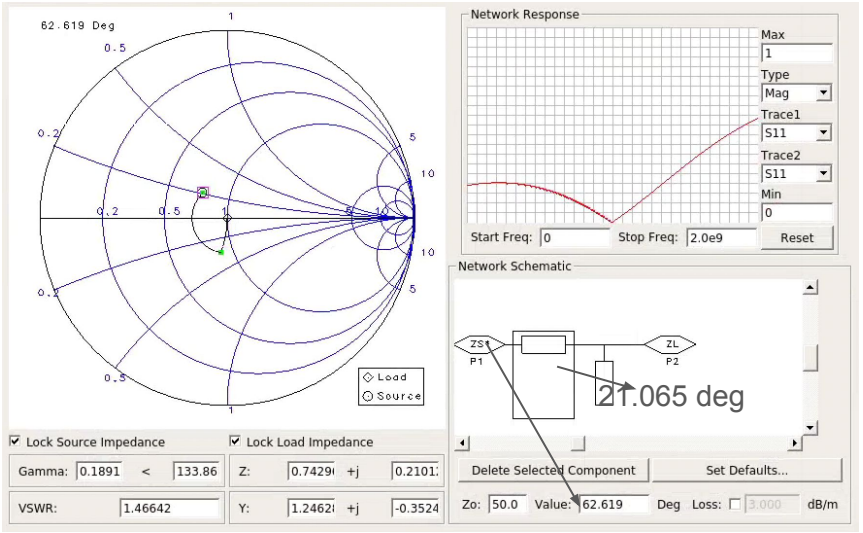
Eqn noise_circles=ns_circle({0.6,0.7,1,1.1,1.23,1.25,1.5,1.73,1.88}, NFmin, Sopt, Rn/50, 201)

Eqn gain_circles=ga_circle(S,{14,13.19,12,11,10}, 201)

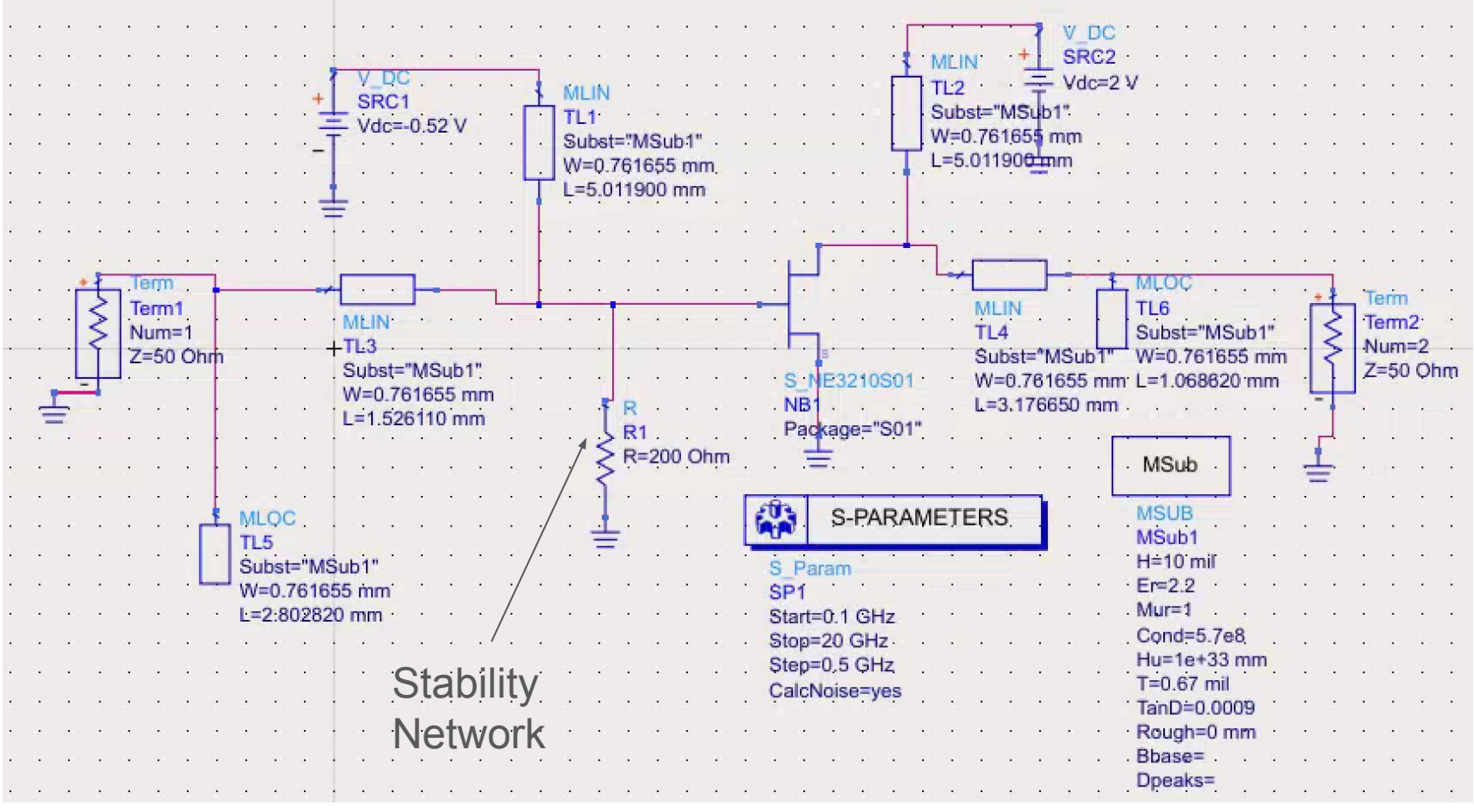


Source vs Load Matching



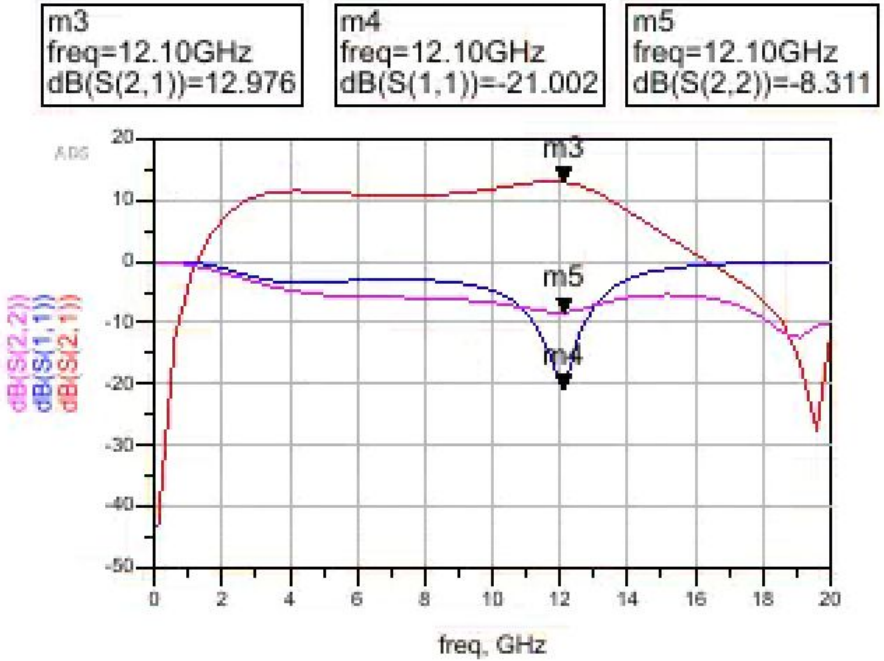


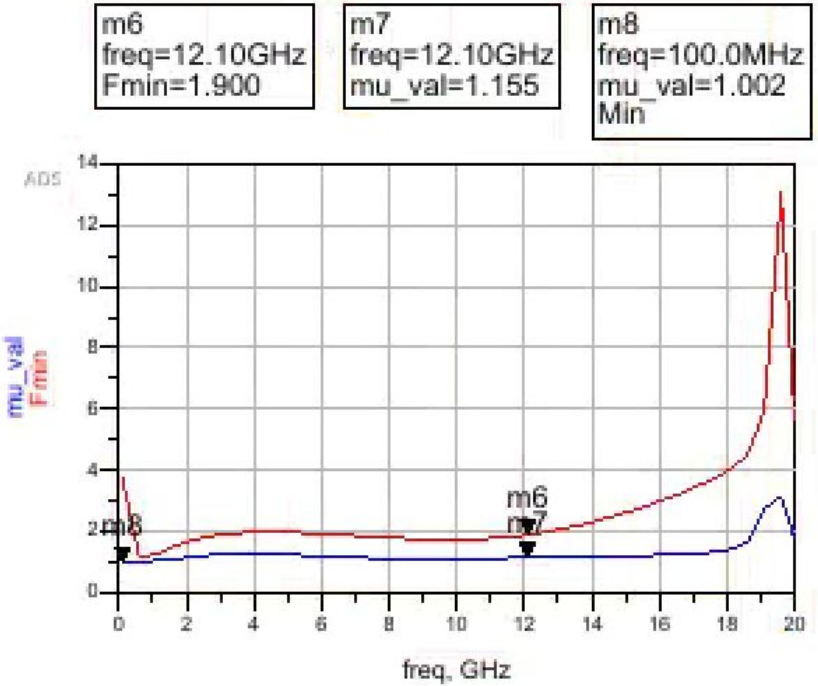
Stage 2 - Matched



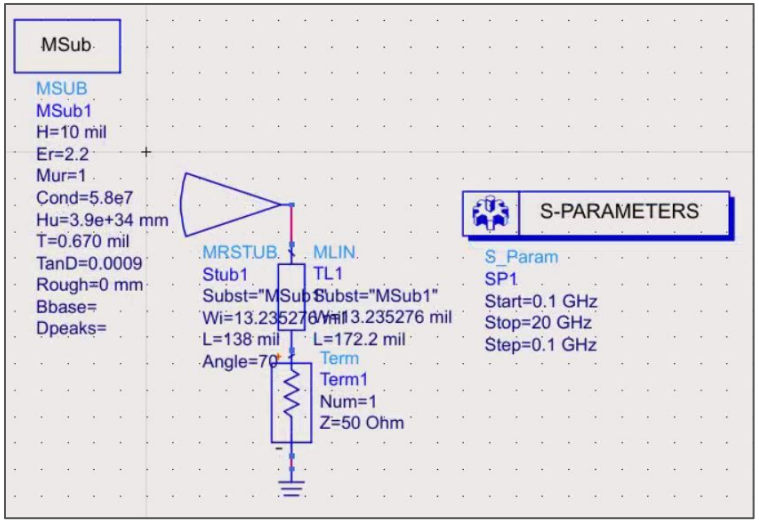
Stage 2 - Results

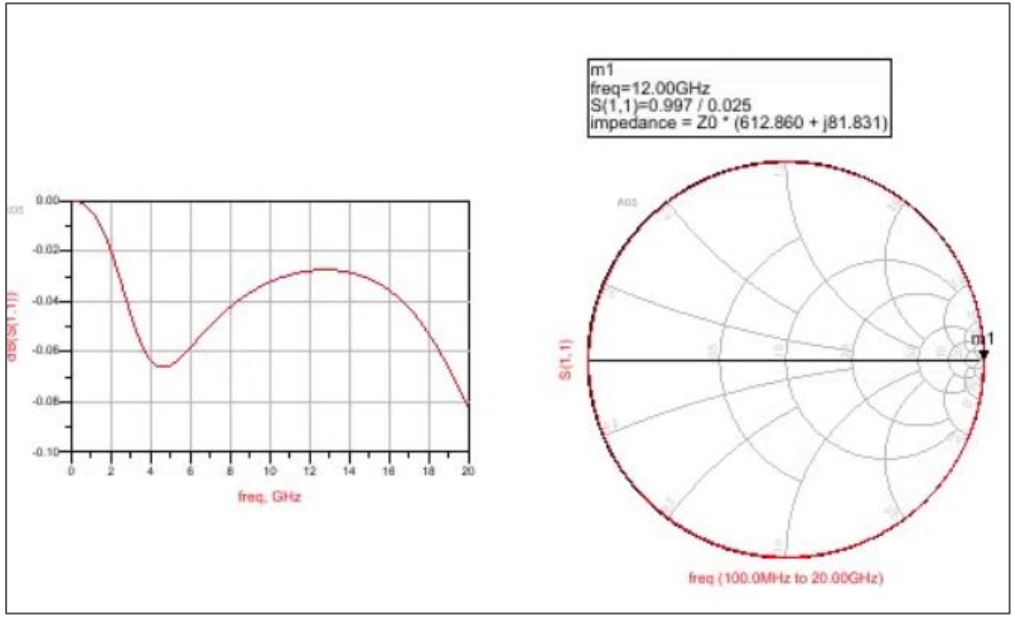
Allowed given the Friis formula



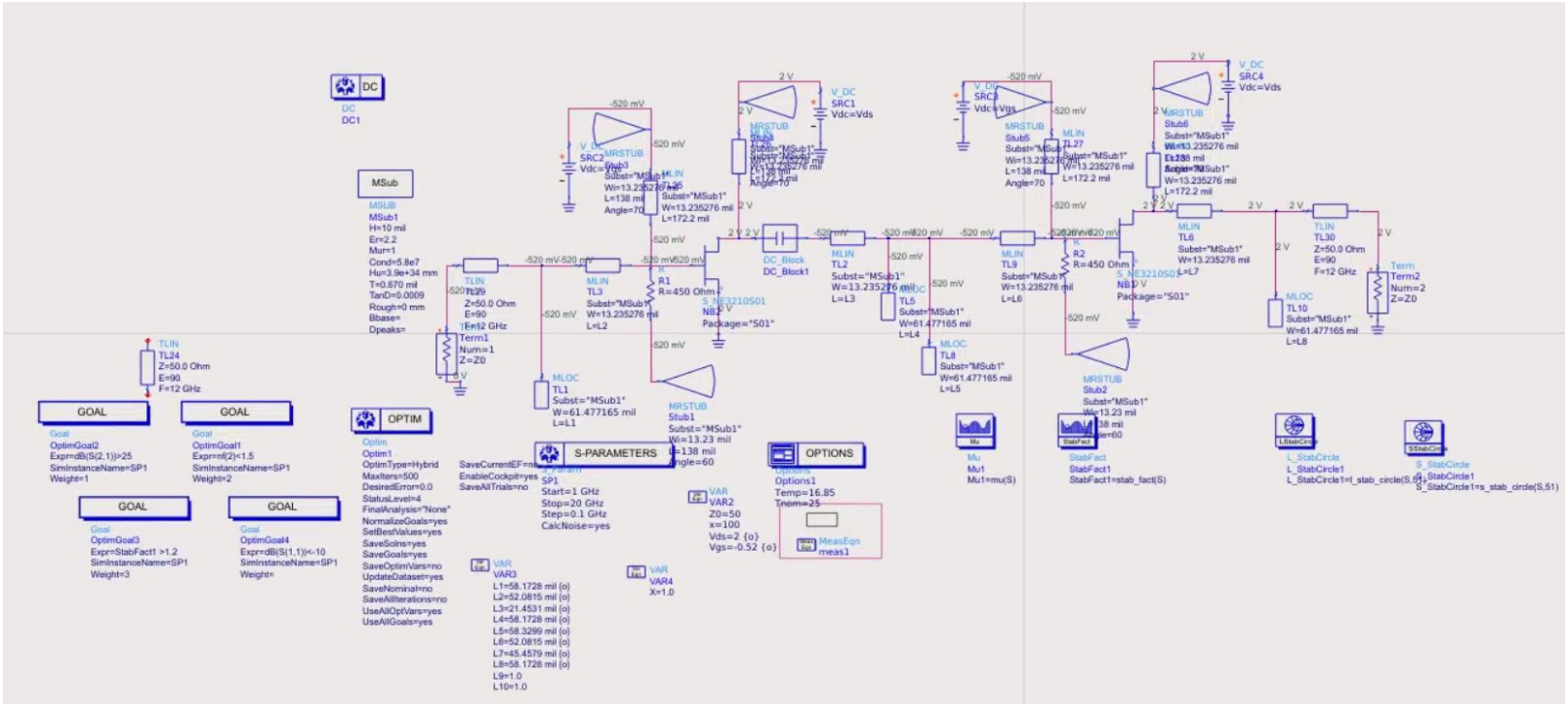


DC feed stage

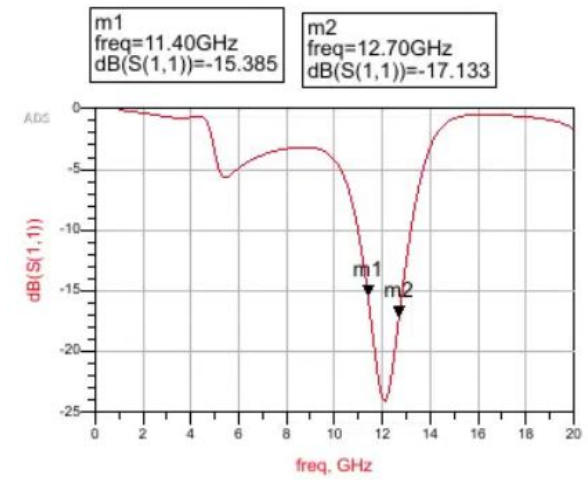


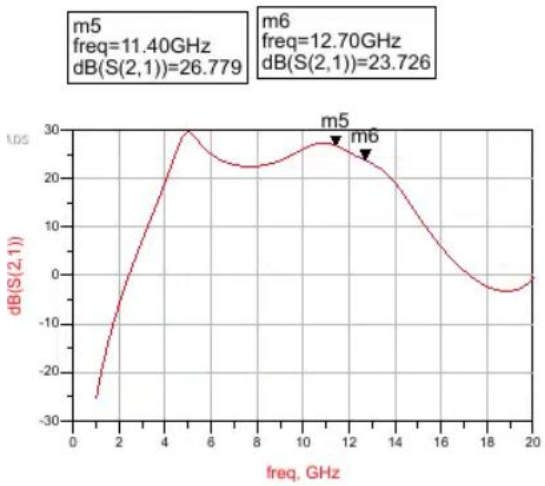


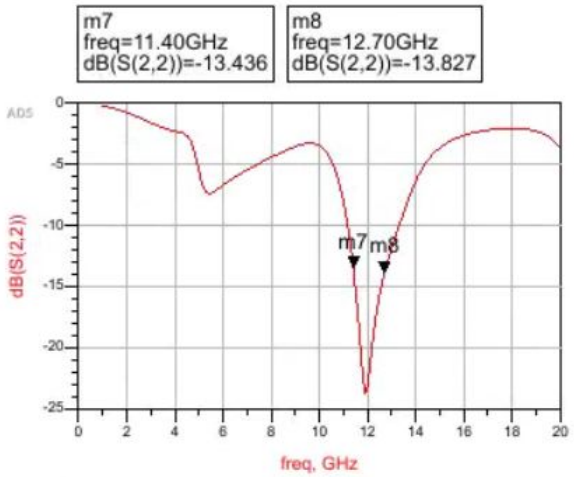
Why the SPICE model doesn’t work for meeting spec

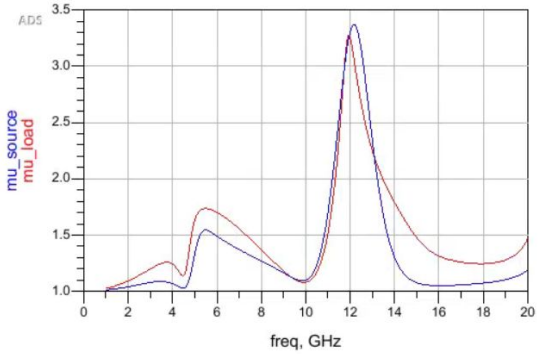


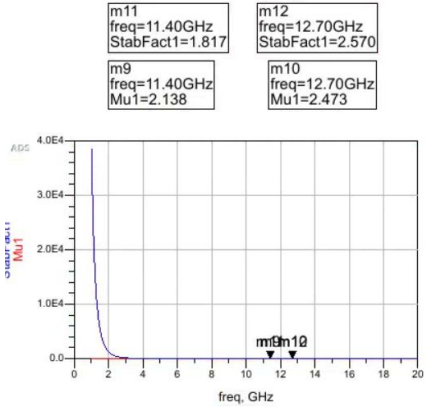
NFmin specifications were not achieved with SPICE Model

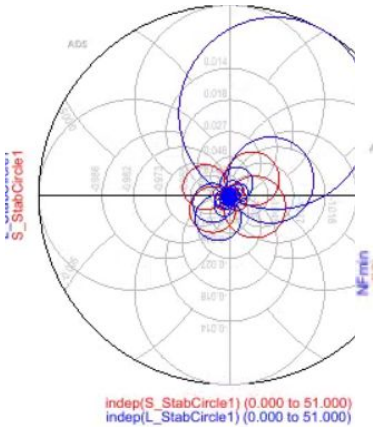


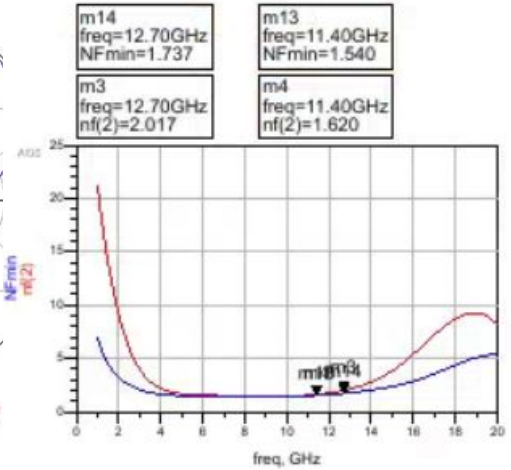




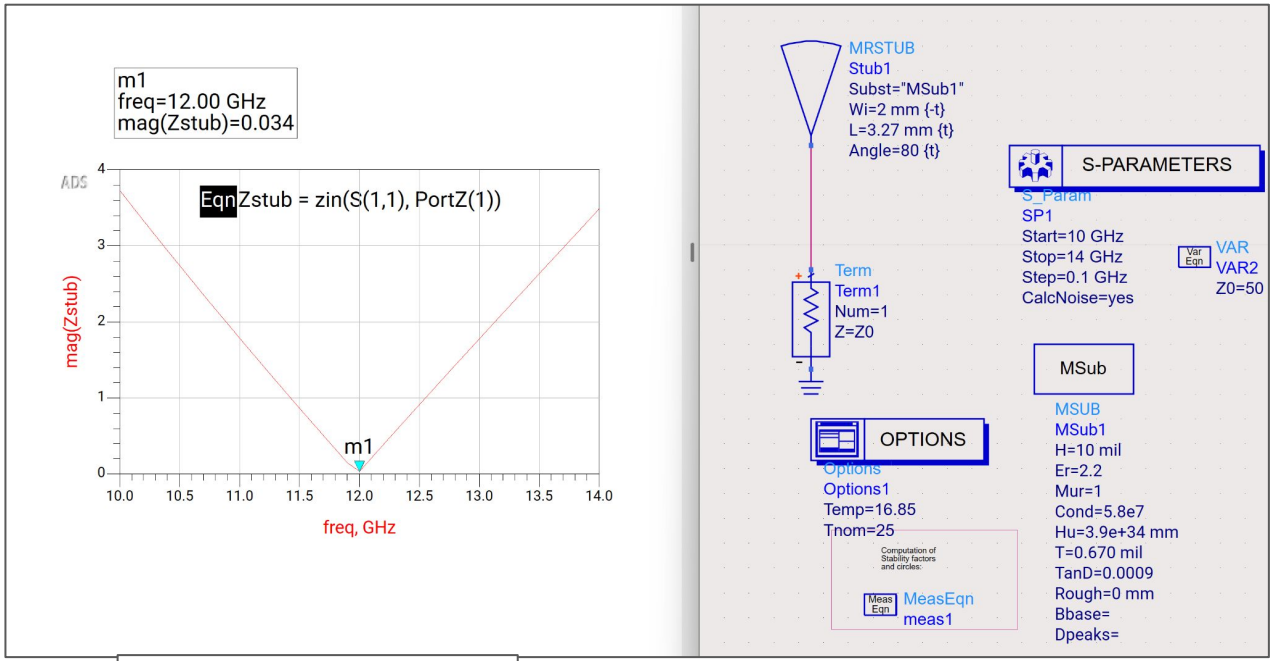


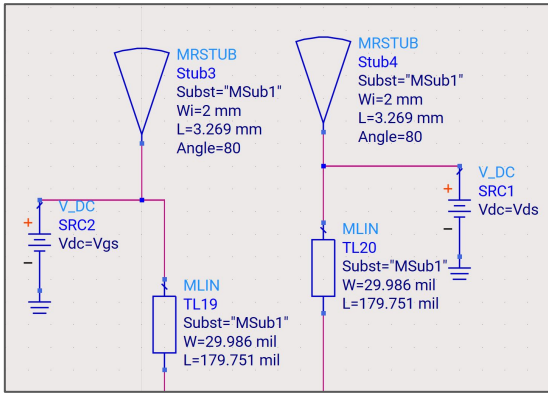






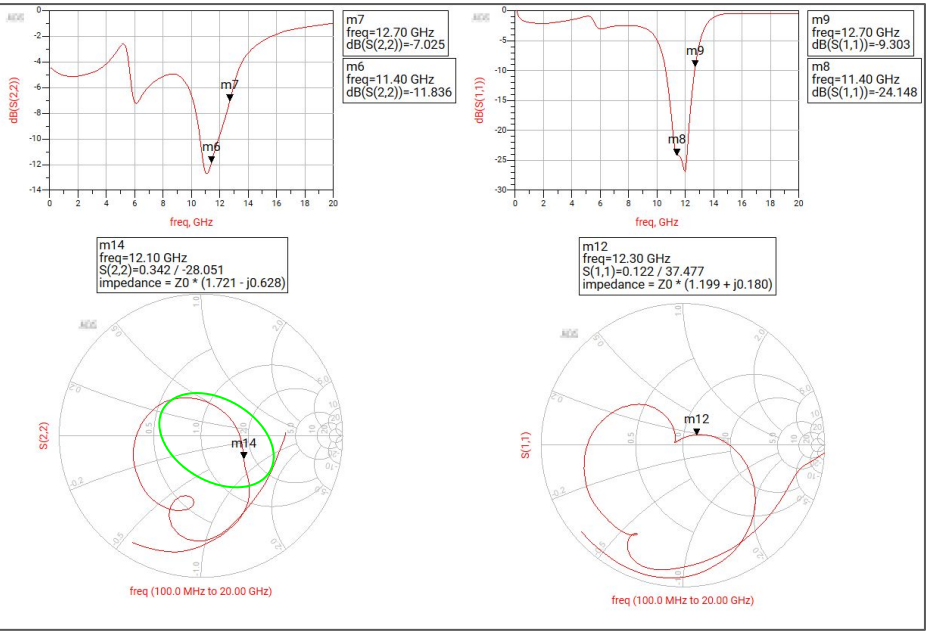
DC feed stage

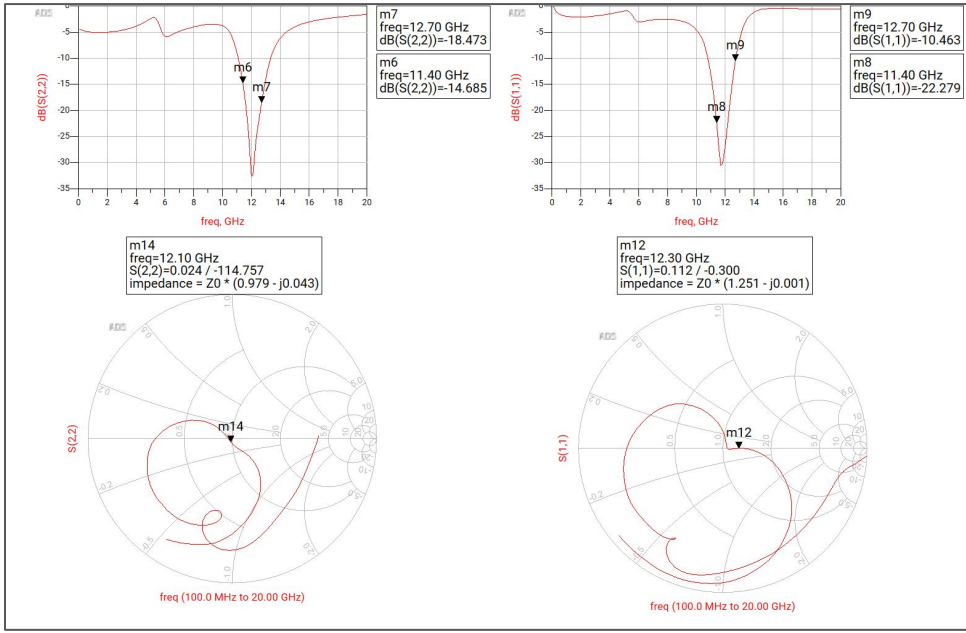




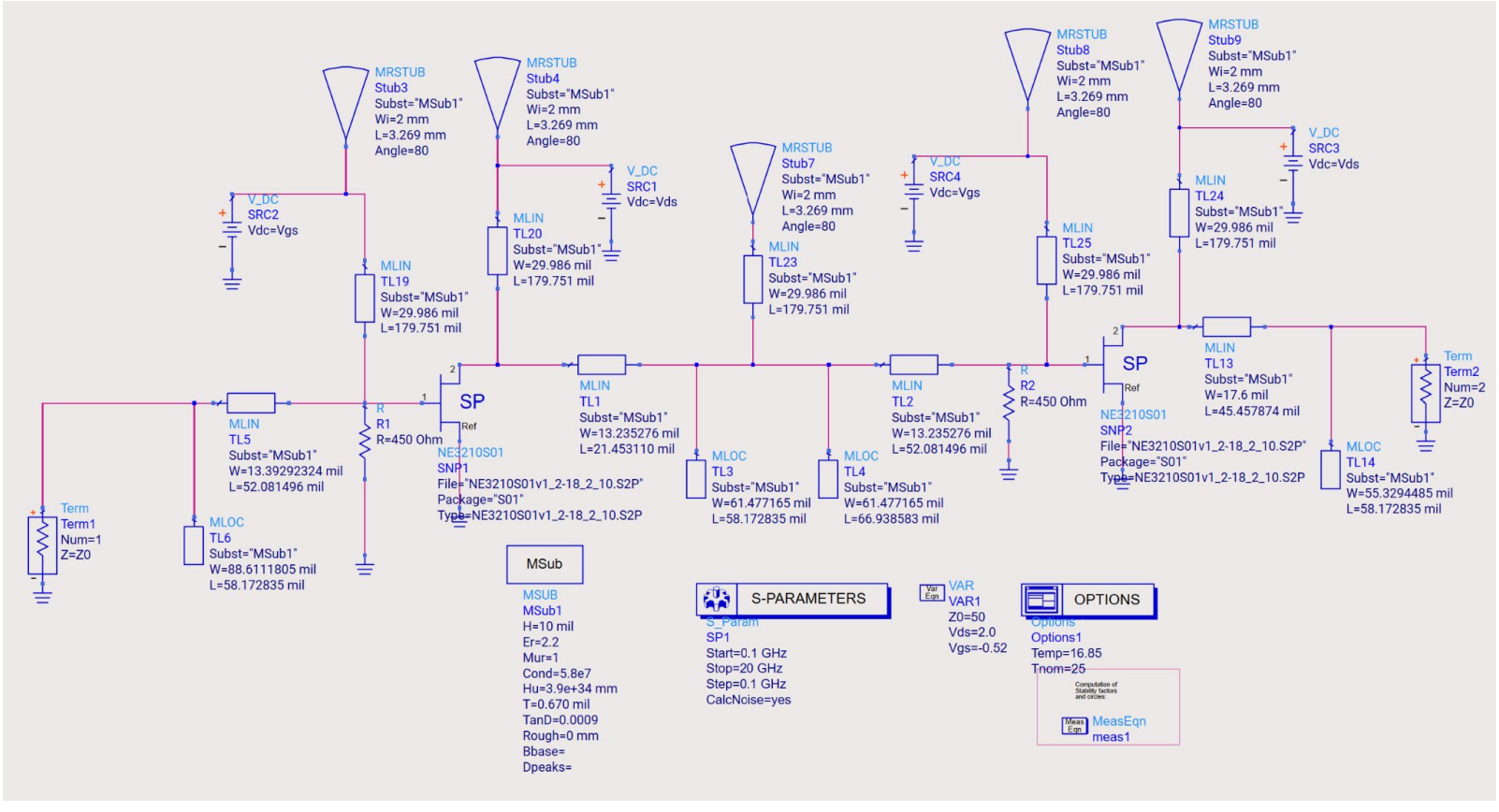
m2
freq=0.0000 Hz
mag(Zstub)=1.124E13

Post DC Feed Fixed Tuning

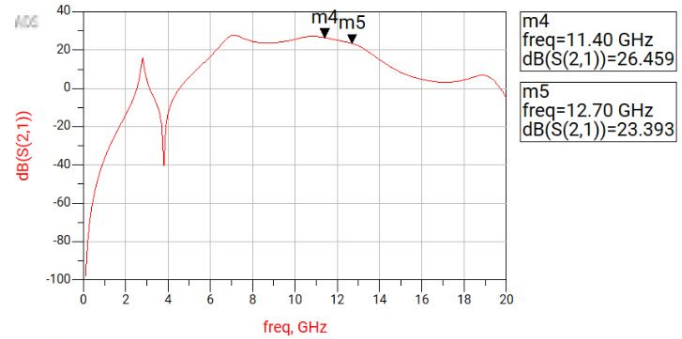


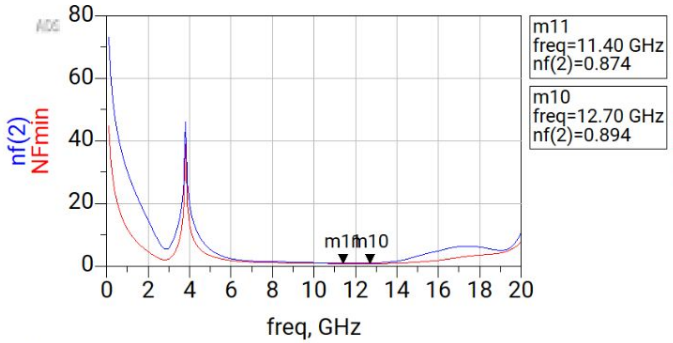


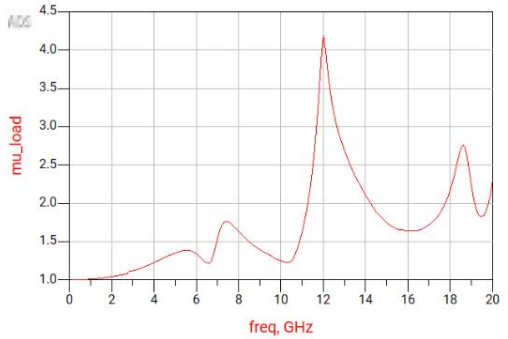
Final SP Schematic

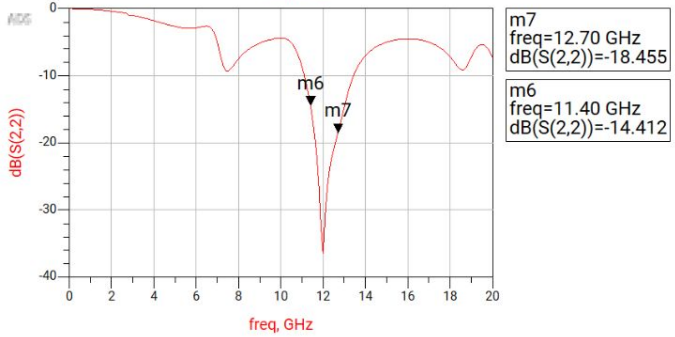


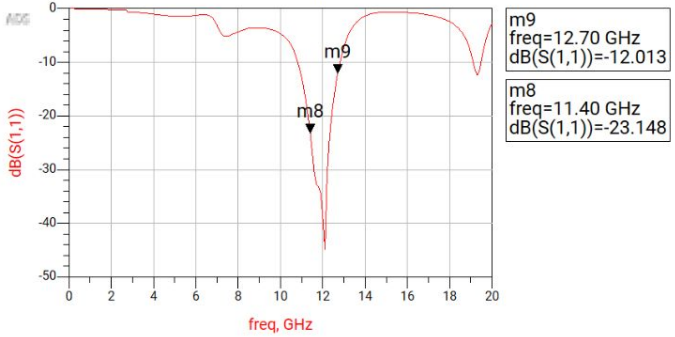
Achieved Specifications

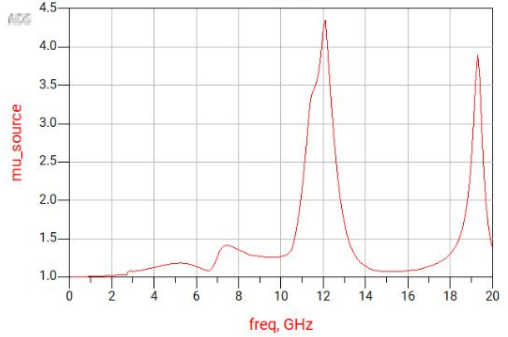








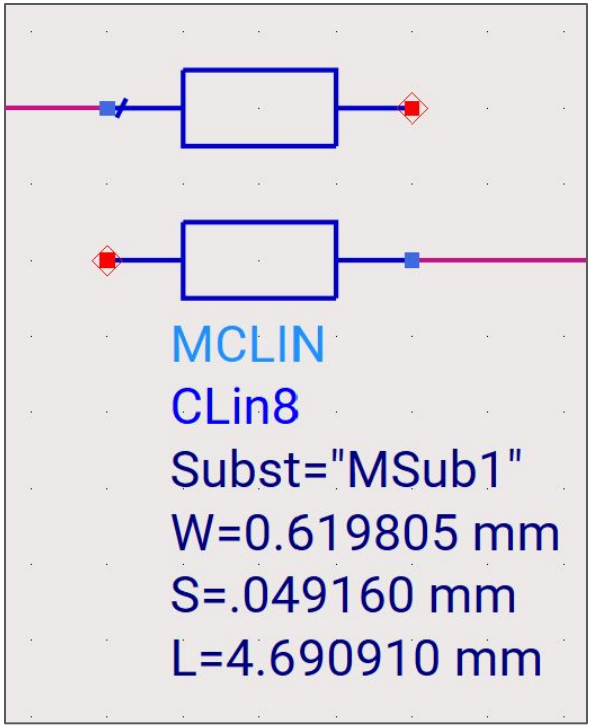


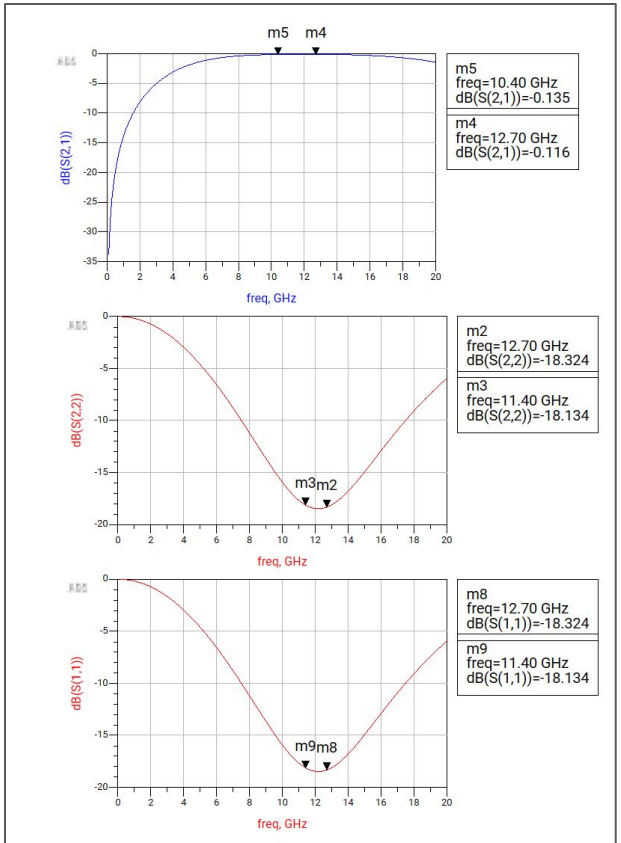


Additional Post Presentation Fixes

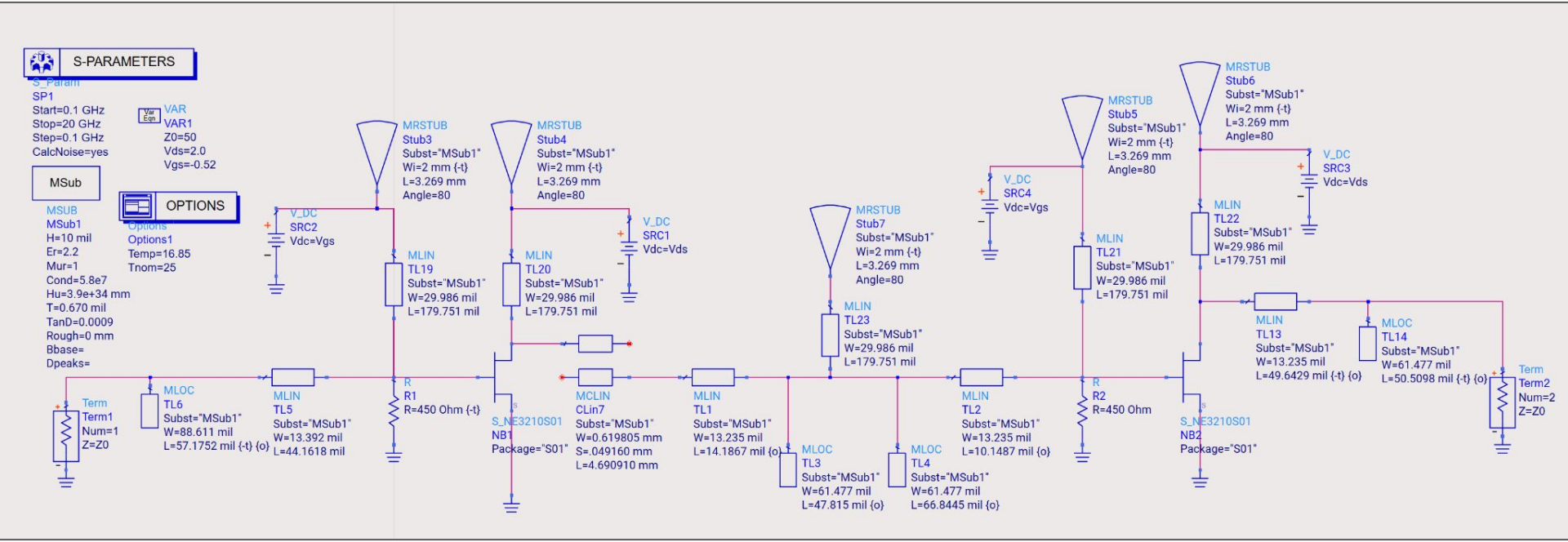
DC Block

- An idea DC Block was replaced with a 12 GHz tuned MCLIN between the LNA stages to maintaining proper biasing
- S21 shows blocking at DC frequencies and passthrough at 12 GHz

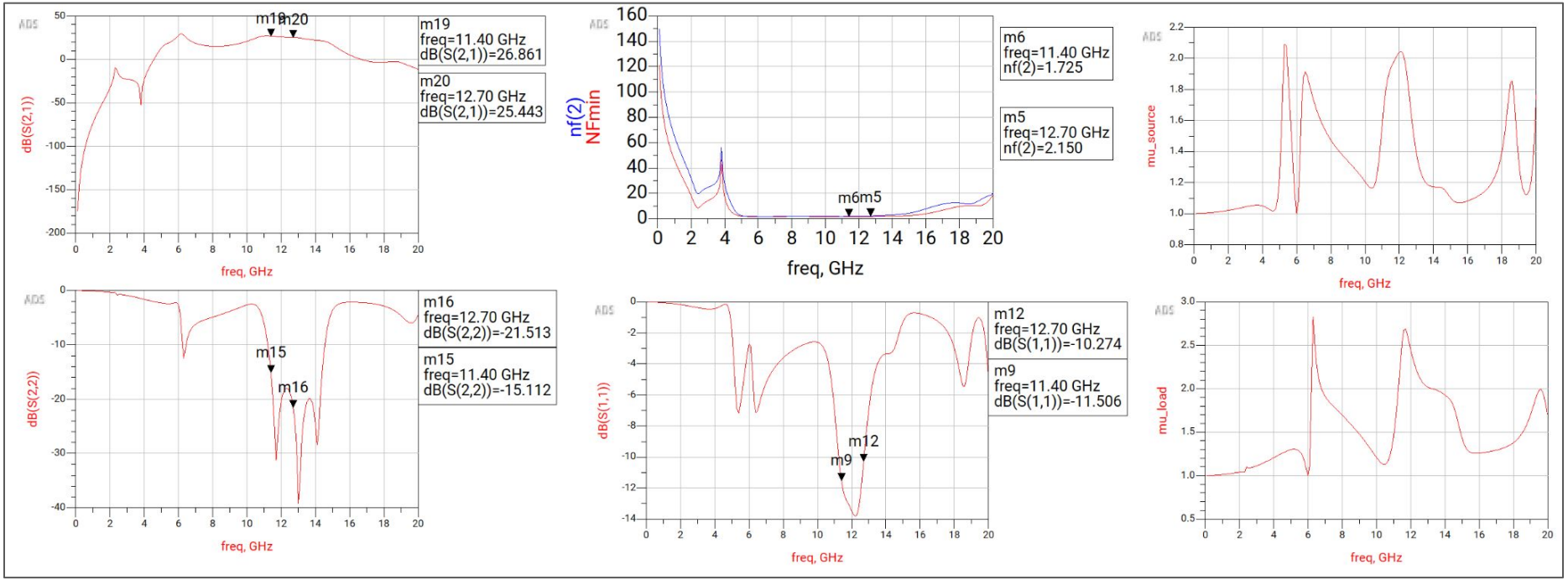




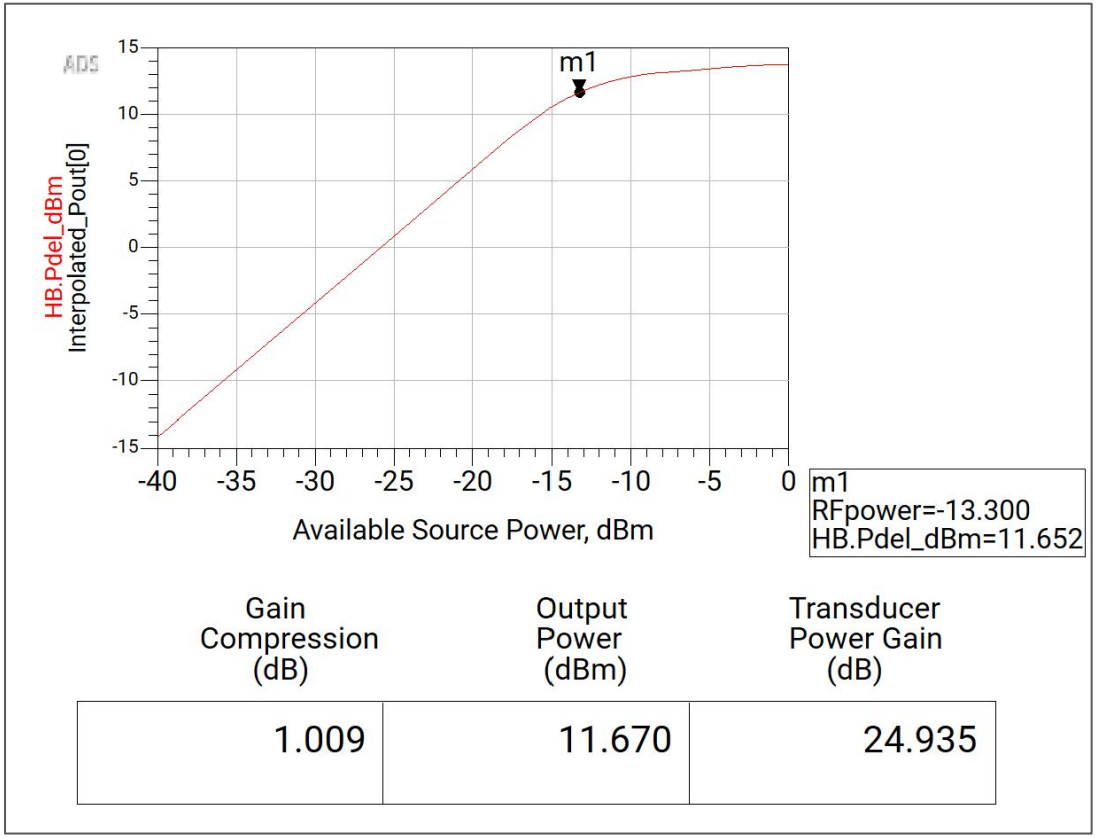
Final Spice Schematic



Achieved Spice Specifications



1dB Compression Point (P1dB)



Gain Compression (dB)	Output Power (dBm)	Transducer Power Gain (dB)
1.009	11.670	24.935

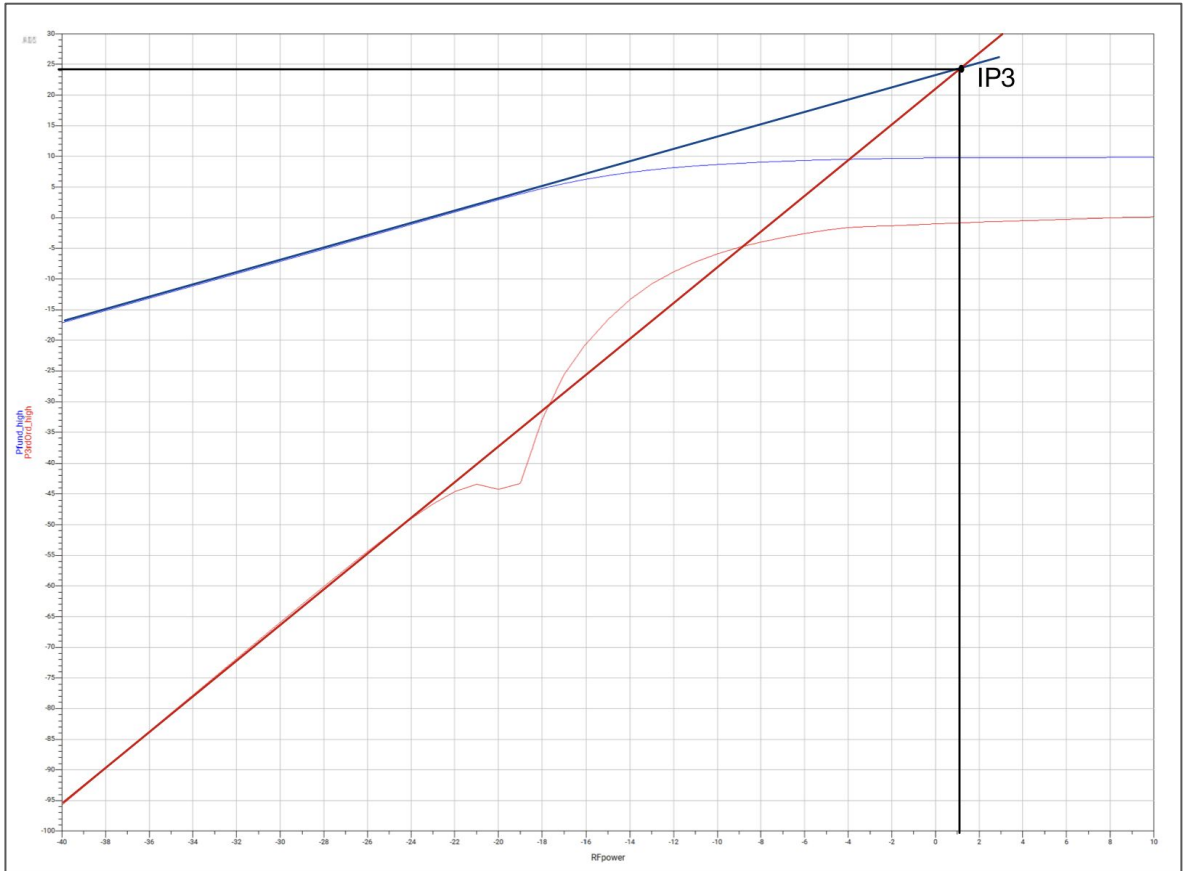
IP1dB = −13.3 dBm

OP1dB = +11.67 dBm

Follows closely with:

OP1dB = (IP1dB + G) − 1 dB

Third-order Intercept Point (IP3)

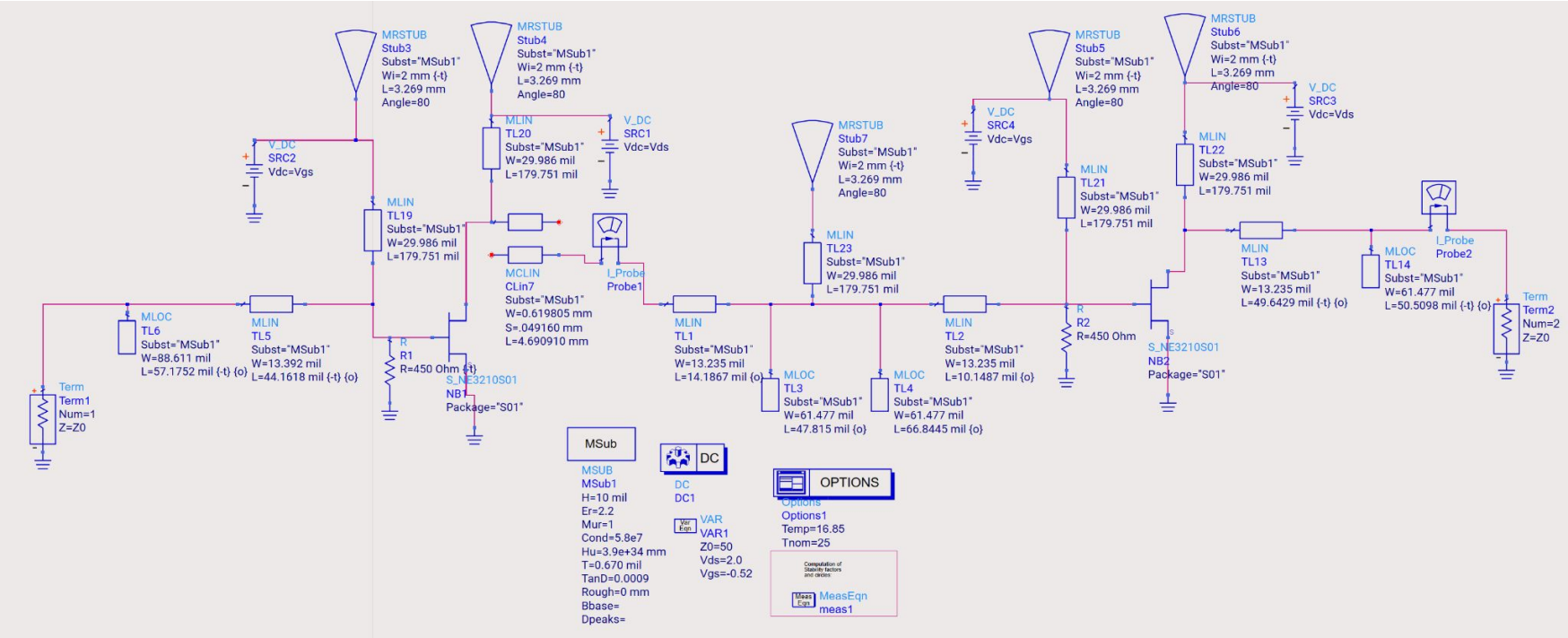


IIP3 = 1 dBm

OIP3= 24 dBm

Notice that OIP3 is approximately IIP3 + Gain in dB

Total DC power = 100mW



Eqn P_dc = Probe1.i*2 + Probe2.i*2

P_dc	Probe1.i	Probe2.i
0.100	-10.13 mA	39.99 mA